REMARKS

In section 3 of the Office Action, the Examiner rejected claims 1-6 under 35 U.S.C. §103(a) as being unpatentable over the Annamalai patent in view of admitted prior art.

The Annamalai patent discloses a process for fabricating a silicon-on-diamond (SOD) structure consisting of a silicon substrate, a thin film of deposited diamond on top of the silicon substrate, and an active silicon layer on top of the diamond film. Devices are fabricated in the active silicon layer. Diamond is used as an electrical insulator as compared with SOI, where silicon dioxide is used as an electrical insulator. The diamond film of the SOD structure has a high electrical resistivity and a high thermal conductivity.

As shown in Figure 1, two epitaxial layers 2 and 3 are grown on a seed silicon wafer 1. The layer 2 is an etch stop layer, and the layer 3 is an undoped silicon layer used to fabricate MOSFETs or bipolar transistors. A diamond layer 4 is deposited on top of the layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer 4, and a silicon handle wafer 6 is bonded on top of the polysilicon layer 5.

The seed silicon wafer 1 is then removed, and the layer 2 is removed. The resulting substrate, turned around, now consists of a silicon substrate 6, a polysilicon layer 5, a diamond layer 4, and an undoped silicon layer 3. Devices can be fabricated in the undoped silicon layer 3. This SOD structure now has a buried diamond layer with silicon on either side.

As shown in Figure 2, a SIMOX wafer 1-2-3 is the starting substrate. The buried oxide 2 is used as an etch stop layer, a diamond film 4 is deposited on top of the silicon layer 3, a thin polysilicon layer 5 is deposited on top of the diamond layer, and a silicon handle wafer 6 is now bonded to the thin polysilicon layer 5. The silicon layer 1 is removed, and the buried silicon dioxide layer 2 is removed. Devices can be fabricated in the thin silicon layer 3.

Figure 3 is used in the patent to show another process of making an SOD structure.

Independent claim 1 is directed to an RF semiconductor device comprising a high resistivity polysilicon handle wafer, a buried oxide layer over the polysilicon handle wafer, and a silicon layer over the buried oxide layer.

The Examiner's argument appears to be that (i) the Annamalai patent discloses the use of high resistivity polysilicon in fabricating semiconductor devices in general, (ii) the present application discloses as "admitted prior art" that high resistivity GaAs has been used in the fabrication of RF semiconductor devices, and (iii) the use of the semiconductor device disclosed in the Annamalai patent in RF applications is, therefore, suggested by the "admitted prior art" since both "references" rely on high resistivity materials. The Examiner then concludes on the basis of this suggestion that the use of the device disclosed in the Annamalai patent as an RF semiconductor device would have been obvious.

However, the Annamalai patent mentions nothing about the resistivity of the polysilicon in the polysilicon layer 5 and does not disclose or suggest that the polysilicon layer 5 is a high resistivity polysilicon layer.

The Annamalai patent does state that the diamond layer 4 has a high resistivity on the order of 10^{16} ohm-cm. However, independent claim 1 requires a high resistivity polysilicon handle wafer, not a high resistivity insulating layer.

Accordingly, since both "references" do not rely on high resistivity materials, there is no suggestion to use the semiconductor device disclosed in the Annamalai patent in RF applications.

Therefore, because there is no suggestion to combine the Annamalai patent and the "admitted prior art," independent claim 1 is not unpatentable over the Annamalai patent in view of "admitted prior art."

Independent claim 3 is directed to an RF semiconductor device comprising a high resistivity polycrystalline layer, a buried oxide layer over the polycrystalline layer, and a silicon layer over the buried oxide layer.

As indicated above, the Annamalai patent does not disclose or suggest that the polysilicon layer 5 is a high resistivity polysilicon layer. The Annamalai patent does state that the diamond layer 4 has a high resistivity on the order of 10^{16} ohm-cm. However, independent claim 3 requires a high resistivity polycrystalline handle wafer, not a high resistivity insulating layer.

Accordingly, there is no suggestion that the device disclosed in the Annamalai patent can be used as an RF semiconductor device. Therefore, independent claim

3 is patentable over the Annamalai patent in view of admitted prior art.

Newly added dependent claims 32 and 34 recite that the high resistivity polysilicon or polycrystalline handle wafer comprises a high resistivity polysilicon or polycrystalline handle wafer having a resistivity ρ greater than 10^6 Ω-cm. The art applied by the Examiner does not show a polysilicon or polycrystalline handle wafer having this resistivity.

Accordingly, dependent claims 32 and 34 are patentable over the Annamalai patent in view of admitted prior art.

Newly added dependent claims 33 and 35 recite that the silicon layer comprises an RF processed silicon layer. The art applied by the Examiner does not show an RF processed silicon layer.

Accordingly, dependent claims 33 and 35 are patentable over the Annamalai patent in view of admitted prior art.

CONCLUSION

In view of the above, examination of the present application is respectfully requested.

Respectfully submitted,

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October 26, 2005